



SIA Roadmap: NTRS 97 Impact on Electronic Packaging

Ron Bracken Ph.D..

Director of Packaging Science

Semiconductor Research Corporation

May 5, 1998



Natl. Tech. Roadmap for Semiconductors

- ◆ Process about 10 Years Old
 - Initiated by The SRC
 - Supported by SIA 1992
- ◆ Goal: Define Projected Needs
 - Suite of Technologies: Each Generation
 - Future Generations
- ◆ Base Projections on Moore's Laws:
 - DRAM Bits/ Chip Increase 4X Every 3 Years
 - Transistors/ cm² @ Double per generation
 - Critical Line Width Reduces Appropriately
 - Processing Cost Reduction 25-30% / Yr. / Function
 - Silicon Processing Cost/ cm² app.. Constant



NTRS: Needs Identification Process

- ◆ Identify Product Needs (ORTC)
- ◆ Reflect Product Needs onto Separate Technologies
- ◆ Recruit Technology Working Groups (TWGS)
- ◆ Roll Up TWG Input into Roadmap
 - Current Process: One generation every two years
 - Roadmap refreshed on that schedule
- ◆ Roadmap Accessible on Web:
 - technology.roadmap@sematech.org
 - Free to Members; non-members can order



Projected Semiconductor Needs

NTRS 1997 Needs Selected Performance Characteristics of Packaged Chips: Microprocessor Product Needs

Yr. of First Product Shipment (Yr. 1)	1997	1999	2001	2003	2006	2009	2012
Feature size (nm)	250	180	150	130	100	70	50
Transistors (M/cm ²) (packed, incl. SRAM)	3.7	6.2	10	18	39	84	180
MPU chip size (mm ²)---Year 1	300	340	385	430	520	620	750
---Year 3 (2nd shrink)	180	205	230	260	310	370	450
Package cost (cents/pin) (Hand-held)(a)	0.70-1.40	0.63-1.26	0.52-1.14	0.52-1.03	0.44-0.89	0.38-0.76	0.33-0.65
(Cost-perf.)(b)	1.40-2.80	1.27-2.52	1.14-2.28	1.03-2.06	0.89-1.77	0.76-1.52	0.65-1.30
Number of package pins/balls (Hand-held)	100-256	117-300	137-352	161-413	205-524	260-666	330-846
(Cost-perf.)	256-600	300-732	352-895	413-1093	524-1476	666-1992	846-2690
Power dissipation (watts) (Hand-held)	1.2	1.4	1.7	2	2.4	2.8	3.2
(Cost-perf.)	28	48	61	75	96	104	109
Minimum logic V _{dd} (volts)	1.8-2.5	1.5-1.8	1.2-1.5	1.2-1.5	0.9-1.2	0.6-0.9	0.5-0.6
On-chip clock (High perf.) (MHz)(c)	600	960	1570	1770	2075	2570	3080
On-chip clock (Cost perf.) (MHz)	350	530	730	930	1100	1470	1830
Chip-to-board clock (High perf.) (MHz)	250	480	785	880	1040	1290	1540

(a) Hand-held- <\$1000 battery-powered products.

(b) Cost Performance- <\$3000 notebook computers, desktop PC's and telecommunications

(c) High Performance- >\$3000 high end workstations, servers, avionics, and the most demanding applications

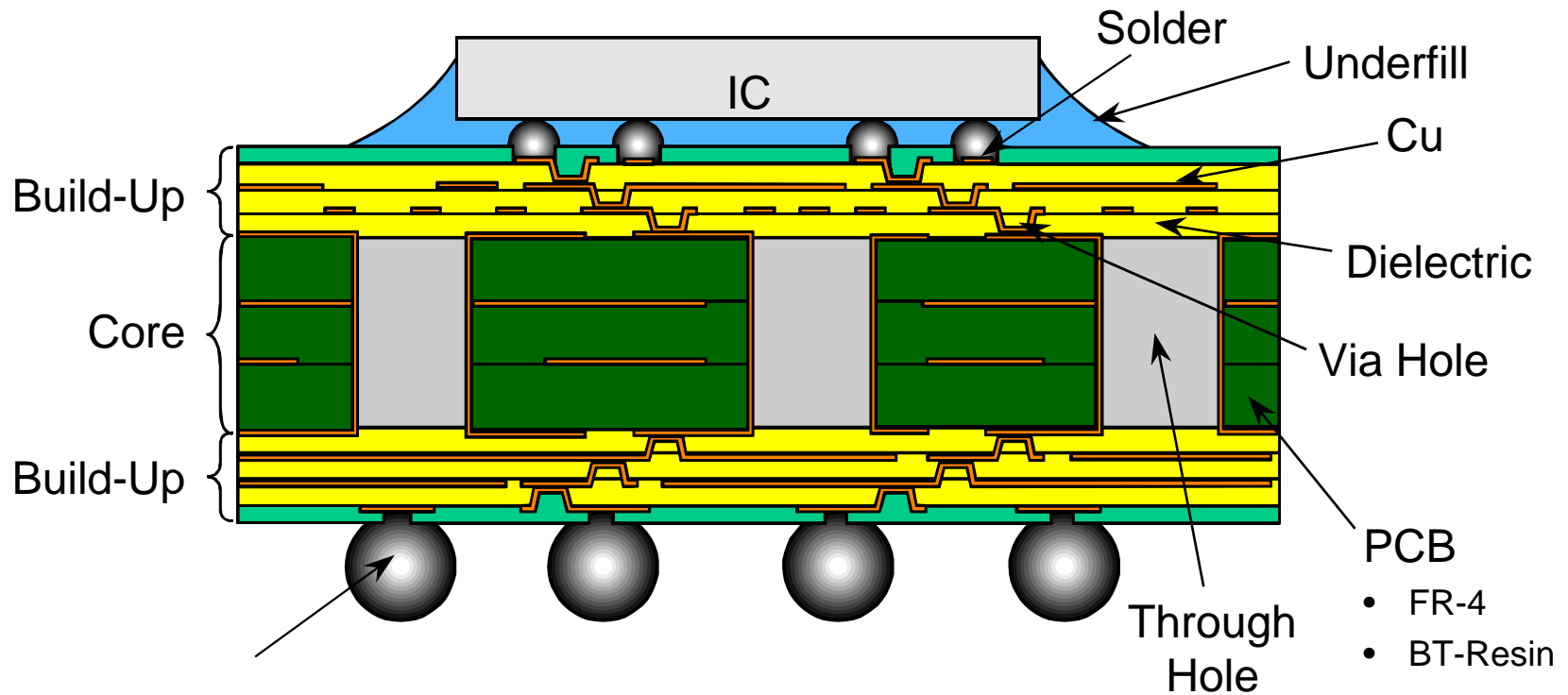
(Excerpt from Table 43 on pp. 135 and 136 of the NTRS[1])



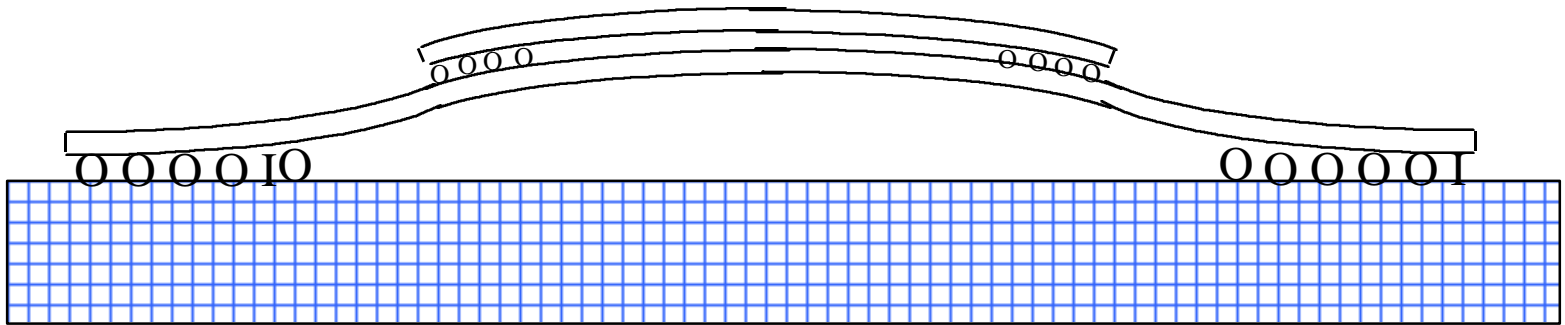
Packaging Environment

Table 3. Performance of Packaged Chips (1997 ORTC)

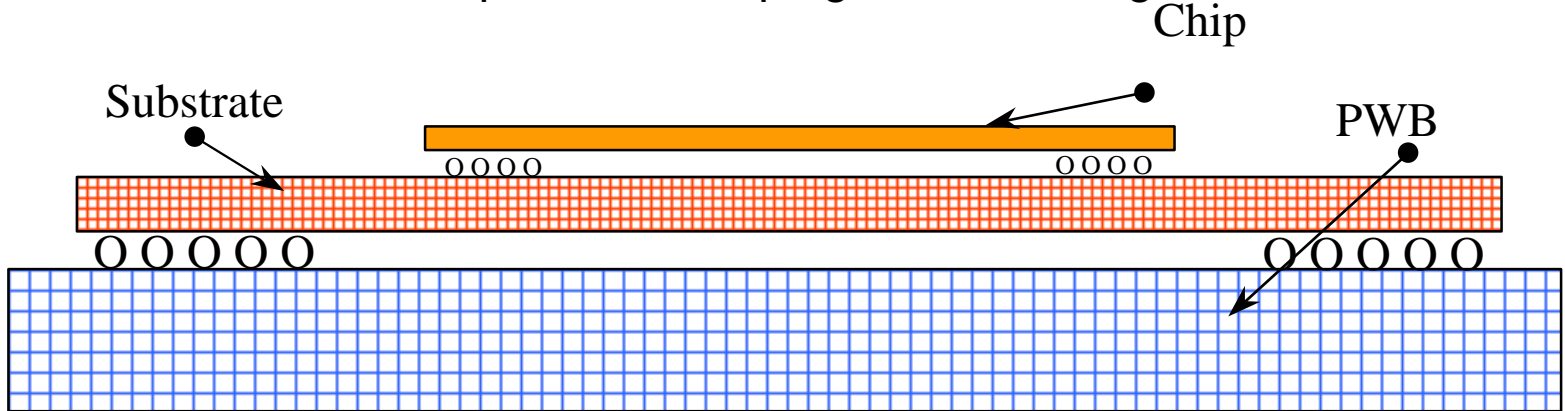
Year of First Product Shipment	1997	1999	2001	2003	2006	2009	2012
Generation Feature Half Pitch (DRAM) nm	250	180	150	130	100	70	50
Isolated Lines (MPU Gates) nm	200	140	120	100	70	50	35
Number of Chip I/O							
Chip to Package (Pads) high perf	1450	2000	2400	3000	4000	5400	7300
Chip to Package (Pads) cost perf	800	975	1195	1460	1970	2655	3585
Number of Package Pins/ Balls							
ASIC (high perf.)	1100	1500	1800	2200	3000	4100	5500
MPU Cost Performance	600	810	900	1100	1500	2000	2700
Cost-performance: cost(cents)/ pin	1.4-2.8	1.25-2.50	1.15-2.30	1.05-2.05	0.90-1.75	0.75-1.50	0.65-1.30
Flip-Chip Pad Pitch (um)	250	180	150	130	100	70	50
Chip Frequency (MHz)							
On-chip local clock; high perf.	750	1250	1500	2100	3500	6000	10000
On-chip across-chip clock; high perf.	750	1200	1400	1600	2000	2500	3000
On-chip across-chip clock; cost perf.	400	600	700	800	1100	1400	1800
Chip to Board (off-chip) speed high perf.	750	1200	1400	1600	2000	2500	3000
Max number of wiring levels	6	6 to 7	7	7	7 to 8	8 to 9	9



- ◆ Semiconductor Companies Pushing Rapid Transition to Area Array Interconnect.
- ◆ Wafer-level Interconnect Materials Changing
- ◆ High Density Substrates Required
- ◆ Thermal Match Important



Low Temperature Warping of Assemblage



Stress-free Assemblage at Bonding or Underfill Temperature

The Flexing of Chip/ Laminate BGA on PWB. Stress borne by underfill polymer the chip and laminate substrate, not solder.



NTRS: Assembly and Packaging

◆ Difficult Challenges

1. Improved Organic Subst. for High I/O F/C
2. Improved Underfills
3. Reliability Limits: High I/O F/C
4. Address Gap between Substrate and Chip Technology
5. Integrated Design Environment
 - Physical, Electrical, Thermal Design
 - Thermo-Mechanical Design
 - Infrastructure
 - Chip/ package/ system integration



NTRS: Assembly and Packaging

◆ Difficult Challenges

6. Chip to Next Level Interconnect

7. Encapsulation and Underfill

8. Single Chip/ Multi-chip Packaging

9. RF and Mixed Signal Packaging



Summary

- ◆ Big Changes Coming in Chip Technology
 - Impact on Packaging will be Profound
- ◆ Strategy of Packaging Sciences
 - Stick to Fundamentals
 - ◆ Materials, Interfaces, Models
 - ◆ Be Aware of Emerging Trends:
- ◆ Seek Coordination of Packaging with other Consortia, National Labs